CLMPTO

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07/29/04

CLAIMS 1-55 CANCELED

--56. (New) A memory device having a normal mode and a test mode, the memory device comprising:

first and second memory arrays, each memory array having memory cells arranged in rows and columns, each column of memory cells having a pair of complementary digit lines;

a pair of complementary data lines;

column select circuitry to concurrently couple at least one pair of complementary digit lines from the first memory array and at least one pair of complementary digit lines from the second memory array to the pair of complementary data lines in response to the memory device being in the test mode;

an amplifier having complementary inputs coupled to the pair of complementary data lines, the complementary inputs of the amplifier coupled to a current source; and

an evaluation circuit coupled to the complementary data lines and generating an output signal having a logic value indicative of a pass-fail condition in accordance with logic levels of the complementary inputs of the amplifier.

57. (New) The memory device of claim 56 wherein the evaluation circuit comprises a two-input NOR gate having each input coupled to a respective one of the complementary data lines.

58. (New) The memory device of claim 56, further comprising first and second latch circuits, the first latch circuit coupled to a first of the complementary data lines and the second latch circuit coupled to a second of the complementary data lines.

59. (New) The memory device of claim 58 wherein the first and second latch circuits comprise: an inverter having an output coupled to a gate of a transistor

a transistor having a source coupled to a respective one of the complementary data lines, a drain coupled to ground, and a gate; and

an inverter having an input coupled to the respective one of the complementary data lines and having an output coupled to the gate.

60. (New) The memory device of claim 56 wherein the amplifier comprises:

first and second amplifier input nodes coupled to a respective one of the complementary data lines;

first and second amplifier output nodes;

first and second pull-up current mirrors, each pull-up current mirror having an input, and first and second outputs, the input of the first pull-up current mirror coupled to the first amplifier input node and the first output of the first pull-up current mirror coupled to the first amplifier output node, and the input of the second pull-up current mirror coupled to the second amplifier input node and the first output of the second pull-up current mirror coupled to the second amplifier output node; and

first and second pull-down current mirrors, each pull-down current mirror having an input and an output, the input of the first pull-down current mirror coupled to the second output of the second pull-up current mirror and the output of the first pull-down current mirror coupled to the first amplifier output node, and the input of the second pull-down current mirror coupled to the second output of the first pull-up current mirror and the output of the second pull-down current mirror coupled to the second amplifier output node.

61. (New) The memory device of claim 56 wherein the column select circuitry comprises a switching circuit coupled between the inputs of the amplifier and the pair of digit lines from the first memory array and between inputs of the amplifier and the pair of digit lines from the second memory array, the switching circuit coupling the inputs of the amplifier to either the pair of digit lines from the first or second memory array when operating in the normal mode, and coupling the inputs of the amplifier to both the pairs of digit lines from the first and second memory arrays when operating in the test mode.

62. (New) The memory device of claim 56, further comprising a third memory array having memory cells arranged in rows and columns, each column of memory cells having a pair of complementary digit lines coupled to complementary data lines through the column select circuitry, the column select circuitry concurrently coupling at least one digit line from the first, second, and third memory arrays.

63. (New) Test compression circuitry for a memory device having first and second arrays of memory cells, the memory cells arranged in rows and columns, each column having a pair of complementary digit lines respectively coupled to a pair of complementary data lines through a switching circuit, the switching circuit concurrently coupling at least one digit line from the first array and at least one digit line from the second array to the complementary data lines concurrently when in a test mode, the test compression circuitry comprising:

an amplifier having a pair of inputs respectively coupled to the complementary data lines, the amplifier driving each of its inputs to either a first or second logic state based on the logic states of all of the complementary digit lines concurrently coupled thereto; and

an evaluation circuit having first and second inputs, each input coupled to a respective input of the amplifier, the evaluation circuit generating an output signal having a logic state indicative of a pass-fail condition in accordance with the logic states of the first and second inputs.

64. (New) The test compression circuitry of claim 63 wherein the amplifier comprises a DC current sensing amplifier having inputs coupled to a pull-up bias.

65. (New) The test compression circuitry of claim 64 wherein the DC current sensing amplifier comprises:

first and second amplifier input nodes coupled to a respective one of the complementary data lines;

first and second amplifier output nodes;

first and second pull-up current mirrors, each pull-up current mirror having an input, and first and second outputs, the input of the first pull-up current mirror coupled to the first amplifier input node and the first output of the first pull-up current mirror coupled to the first amplifier output node, and the input of the second pull-up current mirror coupled to the second amplifier input node and the first output of the second pull-up current mirror coupled to the second amplifier output node; and

first and second pull-down current mirrors, each pull-down current mirror having an input and an output, the input of the first pull-down current mirror coupled to the second output of the second pull-up current mirror and the output of the first pull-down current mirror coupled to the first amplifier output node, and the input of the second pull-down current mirror coupled to the second output of the first pull-up current mirror and the output of the second pull-down current mirror coupled to the second amplifier output node.

66. (New) The test compression circuitry of claim 63, further comprising first and second open-drain transistors coupled a respective one of the complementary data lines to form a wired OR function with the amplifier.

67. (New) The test compression circuitry of claim 63 wherein the evaluation circuit comprises a two-input NOR gate, a first one of the inputs coupled to a first one of the complementary data lines and a second one of the inputs coupled to a second one of the complementary data lines.

68. (New) The test compression circuitry of claim 67 wherein the evaluation circuit further comprises precharge circuitry coupled to each of the inputs of the NOR gate to precharge the inputs to a known logic state.

69. (New) The test compression circuitry of claim 67 wherein the evaluation circuit further comprises latches coupled to each of the inputs of the NOR gate.

70. (New) A memory device having normal and test modes, comprising:

at least three memory arrays, each memory array having memory cells arranged in rows and columns, each column of memory cells having a pair of complementary digit lines;

a pair of complementary data lines to which at least one pair of complementary digit lines from each of the three memory arrays are concurrently coupled during the test mode;

an amplifier having a pair of inputs respectively coupled to the complementary data lines, the amplifier driving each of its inputs to either a first or second logic state based on the logic states of all of the complementary digit lines concurrently coupled thereto; and

an evaluation circuit coupled to the complementary data lines and generating an output signal having a logic state indicative of a pass-fail condition in accordance with logic states of the inputs of the amplifier.

71. (New) The memory device of claim 70, further comprising a first open-drain transistor coupled to a first one of the complementary data lines and a second open-drain transistor coupled to a second one of the complementary data lines, and a wired OR function is formed from the first and second open-drain transistors and the amplifier.

72. (New) The memory device of claim 70 wherein the evaluation circuit comprises a two-input NOR gate, a first one of the inputs coupled to a first one of the complementary data lines and a second one of the inputs coupled to a second one of the complementary data lines.

73. (New) The memory device of claim 72 wherein the evaluation circuit further comprises precharge circuitry coupled to each of the inputs of the NOR gate to precharge the inputs to a known logic state.

74. (New) The memory device of claim 72 wherein the evaluation circuit further comprises latches coupled to each of the inputs of the NOR gate.

75. (New) The memory device of claim 70 wherein the amplifier comprises a DC current sensing amplifier having inputs coupled to a pull-up bias.

76. (New) Test compression circuitry for a memory device having an array of memory cells divided into at least three blocks of memory, the memory cells arranged in rows

and columns, each column having a pair of complementary digit lines, at least one pair of digit lines from each of the three blocks of memory concurrently coupled to a pair of data lines when the memory device is in a test mode, and an amplifier having a pair of inputs respectively coupled to the pair of data lines, the amplifier driving each of its inputs to either a first or second logic state based on the logic states of all of the complementary digit lines concurrently coupled thereto, the test compression circuitry comprising a logic gate having inputs respectively coupled to the complementary data lines and generating an output signal having a logic state indicative of a pass-fail condition in accordance with logic states of the inputs of the amplifier.

77. (New) A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus and adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

first and second memory arrays, each memory array having memory cells arranged in rows and columns, each column of memory cells having a pair of complementary digit lines;

a pair of complementary data lines;

column select circuitry to concurrently couple at least one pair of complementary digit lines from the first memory array and at least one pair of complementary digit lines from the second memory array to the pair of complementary data lines in response to the memory device being in a test mode;

an amplifier having complementary inputs coupled to the pair of complementary data lines, the complementary inputs of the amplifier coupled to a current source; and

an evaluation circuit coupled to the complementary data lines and generating an output signal having a logic value indicative of a pass-fail condition in accordance with logic levels of the complementary inputs of the amplifier.

78. (New) The computer system of claim 77 wherein the evaluation circuit of the memory device comprises a two-input NOR gate having each input coupled to a respective one of the complementary data lines.

79. (New) The computer system of claim 77 wherein the memory device further comprises first and second latch circuits, the first latch circuit coupled to a first of the complementary data lines and the second latch circuit coupled to a second of the complementary data lines.

80. (New) The computer system of claim 79 wherein the first and second latch circuits of the memory device comprise:

an inverter having an output coupled to a gate of a transistor

a transistor having a source coupled to a respective one of the complementary data lines, a drain coupled to ground, and a gate; and

an inverter having an input coupled to the respective one of the complementary data lines and having an output coupled to the gate.

81. (New) The computer system of claim 77 wherein the amplifier of the memory device comprises:

first and second amplifier input nodes coupled to a respective one of the complementary data lines;

first and second amplifier output nodes;

first and second pull-up current mirrors, each pull-up current mirror having an input, and first and second outputs, the input of the first pull-up current mirror coupled to the first amplifier input node and the first output of the first pull-up current mirror coupled to the

first amplifier output node, and the input of the second pull-up current mirror coupled to the second amplifier input node and the first output of the second pull-up current mirror coupled to the second amplifier output node; and

first and second pull-down current mirrors, each pull-down current mirror having an input and an output, the input of the first pull-down current mirror coupled to the second output of the second pull-up current mirror and the output of the first pull-down current mirror coupled to the first amplifier output node, and the input of the second pull-down current mirror coupled to the second output of the first pull-up current mirror and the output of the second pull-down current mirror coupled to the second amplifier output node.

82. (New) The computer system of claim 77 wherein the column select circuitry of the memory device comprises a switching circuit coupled between the inputs of the amplifier and the pair of digit lines from the first memory array and between inputs of the amplifier and the pair of digit lines from the second memory array, the switching circuit coupling the inputs of the amplifier to either the pair of digit lines from the first or second memory array when operating in the normal mode, and coupling the inputs of the amplifier to both the pairs of digit lines from the first and second memory arrays when operating in the test mode.

83. (New) The computer system of claim 77 wherein the memory device further comprises a third memory array having memory cells arranged in rows and columns, each column of memory cells having a pair of complementary digit lines coupled to complementary data lines through the column select circuitry, the column select circuitry concurrently coupling at least one digit line from the first, second, and third memory arrays.

84. (New) A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus and adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

at least three memory arrays, each memory array having memory cells arranged in rows and columns, each column of memory cells having a pair of complementary digit lines;

a pair of complementary data lines to which at least one pair of complementary digit lines from each of the three memory arrays are concurrently coupled during the test mode;

an amplifier having a pair of inputs respectively coupled to the complementary data lines, the amplifier driving each of its inputs to either a first or second logic state based on the logic states of all of the complementary digit lines concurrently coupled thereto; and

an evaluation circuit coupled to the complementary data lines and generating an output signal having a logic state indicative of a pass-fail condition in accordance with logic states of the inputs of the amplifier.

85. (New) The computer system of claim 84 wherein the memory device further comprises a first open-drain transistor coupled to a first one of the complementary data lines and a second open-drain transistor coupled to a second one of the complementary data lines, and a wired OR function is formed from the first and second open-drain transistors and the amplifier.

86. (New) The computer system of claim 84 wherein the evaluation circuit of the memory device comprises a two-input NOR gate, a first one of the inputs coupled to a first one of the complementary data lines and a second one of the inputs coupled to a second one of the complementary data lines.

87. (New) The computer system of claim 86 wherein the evaluation circuit further comprises precharge circuitry coupled to each of the inputs of the NOR gate to precharge the inputs to a known logic state.

88. (New) The computer system of claim 86 wherein the evaluation circuit further comprises latches coupled to each of the inputs of the NOR gate.

89. (New) The computer system of claim 84 wherein the amplifier of the memory device comprises a DC current sensing amplifier having inputs coupled to a pull-up bias.

CLAIMS 90-98 CANCELED